Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT**
2. **GND**
3. **INPUT**

**1**

**DIE ID**

**2**

**L**

**M**

**1**

**4**

**2**

**D**

**.030”**

**.048”**

**3**

**CHIP BACK MUST BE CONNECTED TO GROUND**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LM142D**

**APPROVED BY: DK DIE SIZE .030” X .048” DATE: 11/29/22**

**MFG: NATIONAL SEMI THICKNESS .010” P/N: 78L05**

**DG 10.1.2**

#### Rev B, 7/19/02